instructions to the instruction memory of the transaction generator 20, the host computer 80 programs the various logic devices in the transaction generator using standard software packages available for this purpose. Further, the host computer 80 may exchange data with the data memory of the transaction generator 20, and provide the proper responses to received bus signals to the transaction generator 20 response memory. Alternatively, the transaction generator 20 may be implemented without requiring a host computer 80. The transaction generator 20 may be configured such that necessary programming and control is provided by the system with which it is implemented. In other words, the processor(s) 70 coupled to the processor bus 26, along with the associated control and memory devices 72, 74 coupled to the system bus and other system components (not shown) coupled to the I/O bus 76, may provide the programming and control functions of the host computer.

In The Claims:

Please cancel claims 1, 3-14, 16-19, 21-24, and 31-54 without prejudice. Please add new claims 55-84 as indicated below.

Presentation Of The Claims In A Clean-Unmarked Format

55. (New) A system comprising:

a connector to couple the system to a bus;

an instruction memory to store a plurality of bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases; and

one or more phase generators coupled between the instruction memory and the connector, the one or more phase generators to receive the plurality of bus stimuli

instructions from the instruction memory and to provide a plurality of signals on the bus that represent the predefined sequence of bus transactions.

56. (New) The system of claim 55, wherein the predefined sequence of bus transactions comprises a user specified sequence of bus transactions that has been specified by a user in a high level language.

57. (New) The system of claim 55, wherein the predefined sequence of bus transactions comprises an illegal sequence of bus transactions.

58. (New) The system of claim 55, wherein the predefined sequence of bus transactions is based on a pre-existing simulation stimulus software.

59. (New) The system of claim 55, wherein the predefined sequence of bus transactions is the same as a corresponding predefined sequence of bus transactions specified in a pre-existing simulation stimulus software.

60. (New) The system of claim 55, wherein an instruction of the plurality of bus stimuli instructions comprises an instruction word having a predefined length, the instruction word containing a plurality of predefined segments, each of the plurality of segments to provide instruction to a different portion of the one or more phase generators.

61. (New) The system of claim 55:

wherein an instruction of the plurality of bus stimuli instructions comprises an instruction word having a predefined length, the instruction word having a plurality of predefined segments; and

wherein a first segment of the plurality of predefined segments contains a type of operation, a second segment of the plurality of predefined segments contains an arbitration instruction, a third segment of the plurality of predefined segments

contains address and transaction data, and a fourth segment of the plurality of predefined segments contains a data memory address.

62. (New) The system of claim 55, further comprising a connection interface to a computer system, in which the instruction memory and the one or more phase generators are not implemented, to receive the plurality of predefined bus stimuli instructions.

63. (New) The system of claim 55:

wherein the one or more phase generators includes at least one digital logic device coupled with the instruction memory, and at least one phase engine coupled between the digital logic device and the connector, the at least one digital logic device to generate digital logic representing the plurality of bus stimuli instructions and to provide the digital logic to the at least one phase engine, the at least one phase engine to translate the received digital logic into the plurality of signals and to time providing the signals to the bus; and

further comprising a response memory coupled with the at least one digital logic device to store information relating to a bus transaction phase and a response to a bus stimuli.

64. (New) The system of claim 63:

wherein the connector comprises a connector to connect with a processor socket on a motherboard;

wherein the instruction memory comprises a static random access memory;

wherein the at least one digital logic device comprises a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit; and

wherein the at least one phase engine comprises a logic level translation device.

65. (New) The system of claim 63:

wherein the at least one digital logic device comprises a control logic portion to control phases of a bus transaction including to conduct an arbitration phase and a request phase of the bus transaction, and a data logic portion to exchange data with a bus agent coupled with the bus according to the bus transaction;

further comprising a response memory coupled with the control logic portion to store information relating to a bus transaction phase and a response to a bus stimuli;

further comprising a data memory coupled with the data logic portion to store the exchanged data; and

wherein the at least one phase engine comprises a control phase engine coupled with the control logic portion and a data phase engine coupled with the data logic portion, the control phase engine and the data phase engine to time providing the plurality of signals on the bus.

66. (New) A system comprising:

a connector to couple the system to a bus;

an instruction memory to store a bus stimuli instruction, the instruction having a predefined length, the instruction containing a plurality of segments, the plurality of segments including at least a flow segment and a data segment;

a logic device comprising a flow portion, a request portion, and a data portion that are each coupled with the instruction memory to receive at least a segment of the bus stimuli instruction, the flow portion to receive at least the flow segment from

the instruction memory, and the data portion to receive at least the data segment from the memory, the flow portion, the request portion, and the data portion each comprising a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit, the device to generate digital logic according to the bus stimuli instruction;

a plurality of phase engines including a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine coupled between the logic device and the connector, the system phase engine, the arbitration phase engine, and the request phase engine coupled with the flow portion, the snoop/error phase engine coupled with the request portion, the data phase engine coupled with the data portion, the plurality of phase engines to translate the digital logic received from the logic device into signals and to provide the signals to the bus;

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further comprising a response memory coupled with the flow portion and the request portion to store response information; and

further comprising a data memory coupled with the data portion to store data.

67. (New) The system of claim 66, further comprising a connection interface to a computer system, in which the instruction memory is not implemented, to receive the bus stimuli instruction.

68. (New) The system of claim 66, wherein the bus stimuli instruction is based on a pre-existing simulation stimulus software.

69. (New) A system comprising:

a computer system containing a file that is based on a pre-existing simulation stimulus software and that contains a plurality of bus stimuli instructions that

represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases;

a processor bus;

a transaction generator coupled between the computer system and the bus, the transaction generator containing:

a first connector coupled to the computer system to receive the file;

an instruction memory to store the file;

one or more phase generators coupled between the instruction memory and the first connector, the one or more phase generators to receive the plurality of bus stimuli instructions from the file stored in the instruction memory and to generate a plurality of bus compatible signals that represent the predefined sequence of bus transactions, wherein the one or more phase generators include a logic device selected from the group consisting of a flow programmable gate array and an application specific integrated circuit coupled with the instruction memory to implement the instructions as digital logic and a translation device coupled between the logic device and the bus to translate the digital logic to the plurality of bus compatible signals; and

a second connector coupled to the bus to provide the plurality of bus compatible signals to the bus; and

a component selected from the group consisting of a processor and a chipset attached to the bus to respond to the plurality of bus compatible signals.

70. (New) The system of claim 69, further comprising a logic analyzer coupled with the bus to capture information associated with the response of the component to the plurality of bus compatible signals.

71. (New) The system of claim 69, wherein the plurality of bus stimuli instructions comprise a high level language.

72. (New) A system comprising:

an instruction memory to store a plurality of instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

phase generator means for implementing the plurality of instructions on the bus as the predefined sequence of bus transactions.

73. (New) The system of claim 72, wherein the phase generator means comprises:

logic device means for generating digital logic based on the instructions; and

phase engine means for translating the digital logic into bus logic.

74. (New) The system of claim 72, contained within a second system comprising a computer system coupled with the instruction memory, a bus coupled with the phase generator means, and a component coupled with the bus, wherein the computer system contains a file containing the plurality of instructions, and wherein the component is selected from the group consisting of a processor and a chipset.

75. (New) A method comprising:

coupling a component to a bus;

coupling a device comprising an instruction memory and a phase generator to the bus;

storing a plurality of instructions representing a predefined sequence of bus transactions in the instruction memory;

providing the plurality of instructions from the instruction memory to the phase generator;

using the phase generator to provide signals representing the predefined sequence of bus transactions to the bus according to the plurality of instructions; and

detecting a bug of the component by determining an incorrect response of the component to the predefined sequence of bus transactions.

76. (New) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a processor.

77. (New) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a chipset.

78. (New) The method of claim 75, further comprising generating the plurality of instructions representing the predefined sequence of bus transactions in a high level language based on a simulation stimulus software.

79. (New) An instruction word stored in a device-readable format in a storage device, the instruction word comprising a predefined length containing a plurality of predefined segments, each of the plurality of segments to provide instruction to a different portion of a phase generator of a bus transaction generator.

80. (New) The instruction word of claim 79, wherein a segment of the plurality comprises instruction for digital logic device that is selected from the group

consisting of a field programmable gate array and an application specific integrated circuit.

81. (New) The instruction word of claim 79, wherein the instruction word is based on a user specified bus transaction in a high level language.

82. (New) The instruction word of claim 79, wherein the predefined length is 216 bits.

83. (New) The instruction word of claim 79, wherein a first segment of the plurality of predefined segments contains data identifying a type of operation, a second segment of the plurality of predefined segments contains an arbitration instruction and a request attribute, a third segment of the plurality of predefined segments contains address data and transaction type data, and a fourth segment of the plurality of predefined segments contains a data memory address.

84. (New) The instruction word of claim 79, wherein a segment of the plurality specifies information to transmit to a bus on address and request signal groups in a first packet and a second packet.

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